

PHY 651 – LABORATORY 7 – Rev 1

Introduction to timing circuits

APPLICATIONS OF THE LM555 TIMER

Introduction

In this laboratory, we will use the 555 timer to build a 1 shot circuit to produce a pulse of a given width. You will integrate this electronic circuit construction with some time measurements with Labview.

We will also explore the astable operation of this device, which will allow you to generate waveforms of different duty cycle.

Before starting your work, take some time to familiarize yourself with the LM555 specifications and pinout configuration.

Overview of LM 555 Operation

The LM 555 is a versatile circuit that can perform a variety of timing functions. The basic timing element is a low-pass circuit with a switch S , 2 external resistors R_A and R_B , and an external capacitor C . When the switch S is closed, the capacitor is discharged to 0 voltage with time constant $R_B C$; when S is open, the capacitor charges up to V_{CC} with time constant $(R_A + R_B)C$. In addition, there are two discriminators. The first one switches to logical 1 when the voltage v_{tim} falls **below** $1/3 V_{CC}$, and it activates the SET signal to an internal flip-flop that produces the transition from low to high in the output waveform V_{out} (Pin 3). In addition, this transition makes S open, thus producing the capacitor charge. When the voltage v_{tim} rises above $2/3 V_{CC}$, the flip flop is reset to the 0 quiescent state, and the switch is closed; therefore the capacitor discharges down to 0 with time constant $R_B C$.

In the first activity, R_B is 0; therefore the capacitor discharges very quickly. The trigger produces a low to high transition and, when the capacitor is charged to $2/3 V_{CC}$, the flip-flop is reset and the pulse returns to 0. In the second activity, the capacitor voltage is connected to the trigger input and, when it falls below $1/3 V_{CC}$, it triggers another low to high transition. This process keeps on repeating producing a rectangular waveform

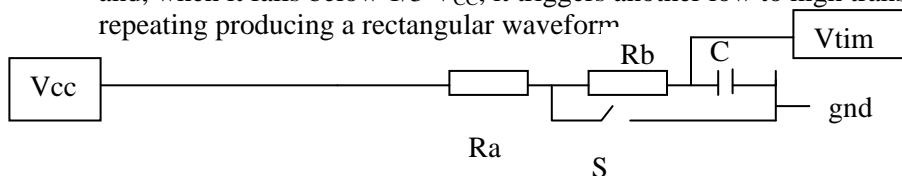


Fig. 1

Activity 1

A timing circuit which has two states, one which can be sustained indefinitely, the other which can be sustained for a certain period of time, after which the output will return spontaneously to the metastable state, is called a MONOSTABLE circuit. If it is forced into this temporary state by an external trigger, it generates a single pulse of fixed duration and then it relapses to its original state. Thus it is also known as “one shot.” In your lab report you should identify possible applications of one shot circuits. An application that you will explore in this laboratory is the generation of a tuneable delay.

Build a one-shot circuit with the 555, using the circuit shown in Figure 1. You should use the +5V supply built in your PB-503 protoboard. To obtain a suitable short triggering signal, you should pass a clock waveform using a square wave of 1KHz frequency, through a 10 μ s high-pass filter returned to +5V. Then the negative spikes fall briefly below the trigger level of $1/3 V_{cc}$.

Study with the oscilloscope the output waveform (pin 3). Observe all the waveforms in the circuit and account for the duration of the pulse.

Write a VI that measures the one shot width.

For your lab report:

Include the measured waveform and explain their relationship and why the width of the output pulse is what you measure.

Include your VI and relate your measurement with Labview with the measurement with the digital scope.

Describe some application for this circuit.

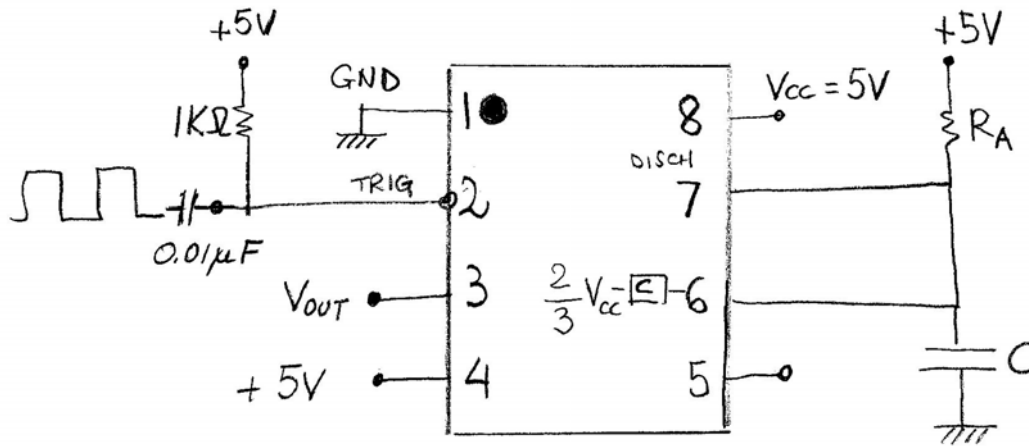


Figure 2

Activity 2

Build a 555 multivibrator selecting R_A , R_B , and C to yield:

A square wave of very nearly 50% duty cycle, and frequency of 0.5 KHz

A negative pulse (about 10 μs long) at V_{out} with a repetition frequency of about 1 KHz.

The astable circuit (multivibrator) is a circuit that continuously switches between the ON and OFF logical levels. We can implement a multivibrator with a 555 circuit but making it trigger itself as soon as the control voltage v_{tim} falls below a trigger level $1/3 V_{\text{cc}}$.

Obviously, it is desirable to cross this level fairly slowly, so as to give the 555 time to trigger, release the discharge switch, and permit to rise smoothly between $1/3 V_{\text{cc}}$ and $2/3 V_{\text{cc}}$. This implies that a non 0 R_B should be used. The time constants of the rise and fall of v_{tim} are $\tau_{\text{rise}} = (R_A + R_B)C$ and $\tau_{\text{fall}} = R_B C$.

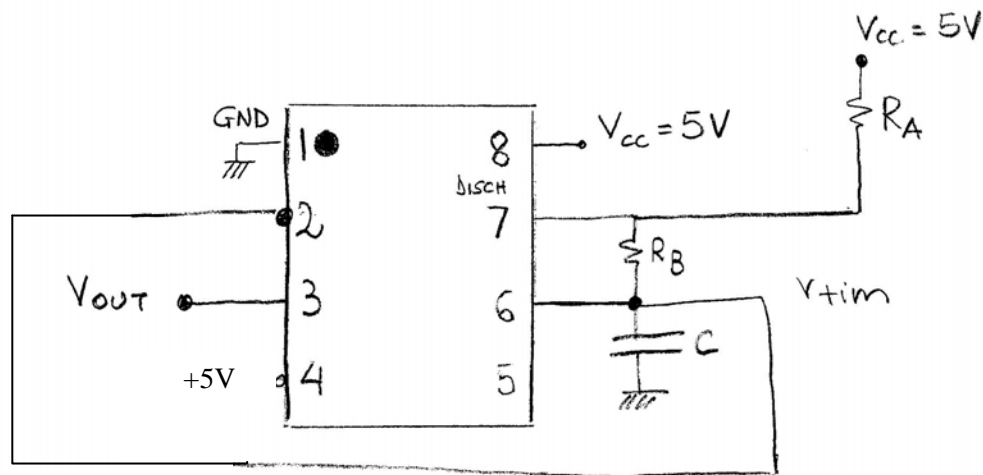


Figure 3

Note on Measuring Times with Labview

An alternative to using Labview as an oscilloscope is the use of the “COUNTER FUNCTION” provided by the NI e6023/4 DAQ boards. These boards use the National Instruments DAQ-STC system timing controller for time-related functions. The DAQ-STC consists of three timing groups that control analog input, analog output, and general-purpose counter/timer functions. The last group is useful to perform time measurements. The general purpose counter/timer functions are started by the leading edge of the corresponding gate and can be configured to make a variety of measurements. They can use an internal clock (20 MHz/100 KHz) or an external source.

I am attaching some relevant information from the NI6023 manual.

GPCTR0_GATE Signal

Any PFI pin can externally input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, the GPCTR0_GATE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform actions such as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR0_GATE signal reflects the actual gate signal connected to general-purpose counter 0. This is true even if the gate is being externally generated by another PFI. This output is set to tri-state at startup. Figure 4-36 shows the timing requirements for the GPCTR0_GATE signal.

Figure 4-36. GPCTR0_GATE Signal Timing in Edge-Detection Mode

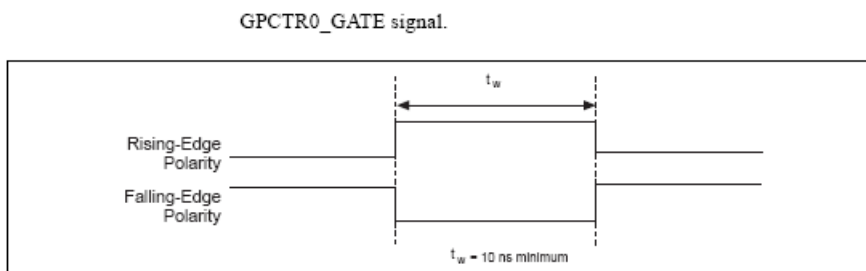


Figure 4-36. GPCTR0_GATE Signal Timing in Edge-Detection Mode

We will explore more details of timing functions in your DAQ in the next lab session.